AMENDMENTS TO THE CLAIMS

Claim 1 (Previously Presented) A ferroelectric memory device comprising a plurality of memory cells, each memory cell including a respective memory cell transistor and a respective memory cell capacitor, such that the ferroelectric memory device includes a plurality of memory cell transistors and a plurality of memory cell capacitors,

wherein each respective memory cell capacitor comprises:

a lower electrode connected to a bit line via the respective memory cell transistor;

a ferroelectric layer formed on an upper surface of the lower electrode and having a width direction that is the same as a width direction of the lower electrode; and

an upper electrode formed on an upper surface of the ferroelectric layer and having a width direction that is the same as the width direction of the lower electrode,

wherein the lower electrodes of the memory cell capacitors are independent from one another,

wherein the upper electrodes of the memory cell capacitors form a continuous plate electrode covering the lower electrodes of the memory cell capacitors, and

wherein the width of each respective upper electrode is narrower than the width of each respective ferroelectric layer.

Claim 2 (Previously Presented) The ferroelectric memory device as defined in Claim 1 wherein the width of each respective lower electrode is narrower than the width of each respective ferroelectric layer.

Claim 3 (Previously Presented) The ferroelectric memory device as defined in Claim 2

wherein the width of each respective upper electrode and the width of each respective lower electrode are substantially the same, and

wherein a position of each respective upper electrode in the width direction and a position of each respective lower electrode in the width direction are substantially aligned.

Claim 4 (Previously Presented) The ferroelectric memory device as defined in Claim 2

wherein the width of each respective upper electrode and the width of each respective lower electrode are substantially the same, and

wherein a position of each respective upper electrode in the width direction and a position of each respective lower electrode in the width direction are different.

Claim 5 (Previously Presented) A ferroelectric memory device comprising a plurality of memory cells, each memory cell including a respective memory cell transistor and a respective memory cell capacitor, such that the ferroelectric memory device includes a plurality of memory cell transistors and a plurality of memory cell capacitors,

wherein each respective memory cell capacitor comprises:

a lower electrode connected to a bit line via the respective memory cell transistor;

a ferroelectric layer formed on an upper surface of the lower electrode; and

an upper electrode formed on an upper surface of the ferroelectric layer,

wherein the lower electrodes of the memory cell capacitors are independent from one another,

wherein the upper electrodes of the memory cell capacitors form a continuous plate electrode covering the lower electrodes of the memory cell capacitors,

wherein a position of one edge of each respective upper electrode substantially aligns with a position of one edge of each respective ferroelectric layer, and

wherein another edge of each respective upper electrode is inwardly located at a position relative to another edge of each respective ferroelectric layer.

Claim 6 (Previously Presented) The ferroelectric memory device as defined in Claim 5 wherein one edge of each respective lower electrode is inwardly located at a position relative to one edge of each respective upper electrode, and a position of another edge of each respective lower electrode substantially aligns with a position of another edge of each respective upper electrode.

Claim 7 (Previously Presented) A ferroelectric memory device comprising a plurality of memory cells, each memory cell including a respective memory cell transistor and a respective memory cell capacitor, such that the ferroelectric memory device includes a plurality of memory cell transistors and a plurality of memory cell capacitors,

wherein each respective memory cell capacitor comprises:

a lower electrode connected to a bit line via the respective memory cell transistor;

a ferroelectric layer formed on an upper surface of the lower electrode; and

an upper electrode formed on an upper surface of the ferroelectric layer,

wherein the lower electrodes of the memory cell capacitors are independent from one another,

wherein the upper electrodes of the memory cell capacitors form a continuous plate electrode covering the lower electrodes of the memory cell capacitors,

wherein a position of one edge of each respective upper electrode substantially aligns with a position of one edge of each respective ferroelectric layer,

wherein another edge of each respective upper electrode is inwardly located at a position relative to another edge of each respective ferroelectric layer, and

wherein one edge of each respective lower electrode is inwardly located at a position relative to one edge of each respective ferroelectric layer, and a position of another edge of each respective lower electrode substantially aligns with a position of another edge of each respective ferroelectric layer.

Claim 8 (Previously Presented) The ferroelectric memory device as defined in Claim 1 wherein each respective lower electrode includes a groove-type structure.

Claim 9 (Previously Presented) The ferroelectric memory device as defined in Claim 8 wherein a groove formed in each respective lower electrode extends along a direction that is parallel to a direction along which each respective upper electrode extends.

Claim 10 (Previously Presented) The ferroelectric memory device as defined in Claim 8 wherein a direction along which a groove formed in each respective lower electrode extends is perpendicular to a direction along which each respective upper electrode extends.

Claims 11-15 (Cancelled)